

Compatibility and usage testing of the HT2015 HART Modem with a 2.7V power supply.

The Smar Research HT2015 is a field-proven mixed signal HART modem. Combining a digital modem core with an array of analog amplifier and comparators, the HT2015 is designed to be a compact, reliable and easy to implement HART modem solution for industrial applications. The standard voltage levels for microprocessor based designs using the HT2015 is generally either 3.3 volts or 5 volts. The HT2015 is designed to work at these levels, allowing for easy interconnection with many popular microprocessors on the market. In these cases, the interconnection of the HT2015 to the microprocessor and surrounding HART circuitry is a straightforward exercise as detailed in the standard HT2015 documentation. For more details on implementing the HT2015 with these standard voltage levels, please refer to the HT2015 Datasheet and HT2015 Application Notes.

Besides the standard voltage range of 3.3 to 5 volts, the HT2015 can also run on voltages down to 2.7 volts. If your design requires an atypical power supply voltage, the HT2015 can still be used. In order to test and approve the HT2015 for usage down to 2.7 volts, the following testing scheme was implemented and observed.

For testing purposes, a typical HT2015 circuit design was employed using the principles and practices explained in the HT2015 Datasheet and HT2015 Application Notes. In replacement of the typical 3.3 or 5 volts, a power supply of 2.7 volts was applied to V_{DD} . A typical 3.3 volt microprocessor was used to interface to the HT2015. In order to isolate the 3.3V microprocessor power supply from the 2.7V HT2015 power supply, a level translator was implemented between all microprocessor and HT2015 UART signals. A dual-bit dual-supply bus transceiver from Texas Instruments, SN74LVC2T45, was used to accomplish this level translation.

This circuit was then connected to a typical HART network and tested for communication errors. The HT2015 underwent communication testing and logging for 24 hours subjected to temperature ranges of -40° to $+85^{\circ}\text{C}$. The HT2015 design was set to receive and transmit communication messages to a HART secondary mater device constantly during this 24 hour period. The communications of the HT2015 design were monitored for any errors. After the 24 hour testing period was completed, the test design exhibited 0 errors over the 24 hour period under any of the subjected temperature range.

This test has been done as a proof of concept and was used to successfully verify full compatibility of the HT2015 with power supply voltages down to 2.7 volts. An overview diagram of the test design can be seen in Figure 1.

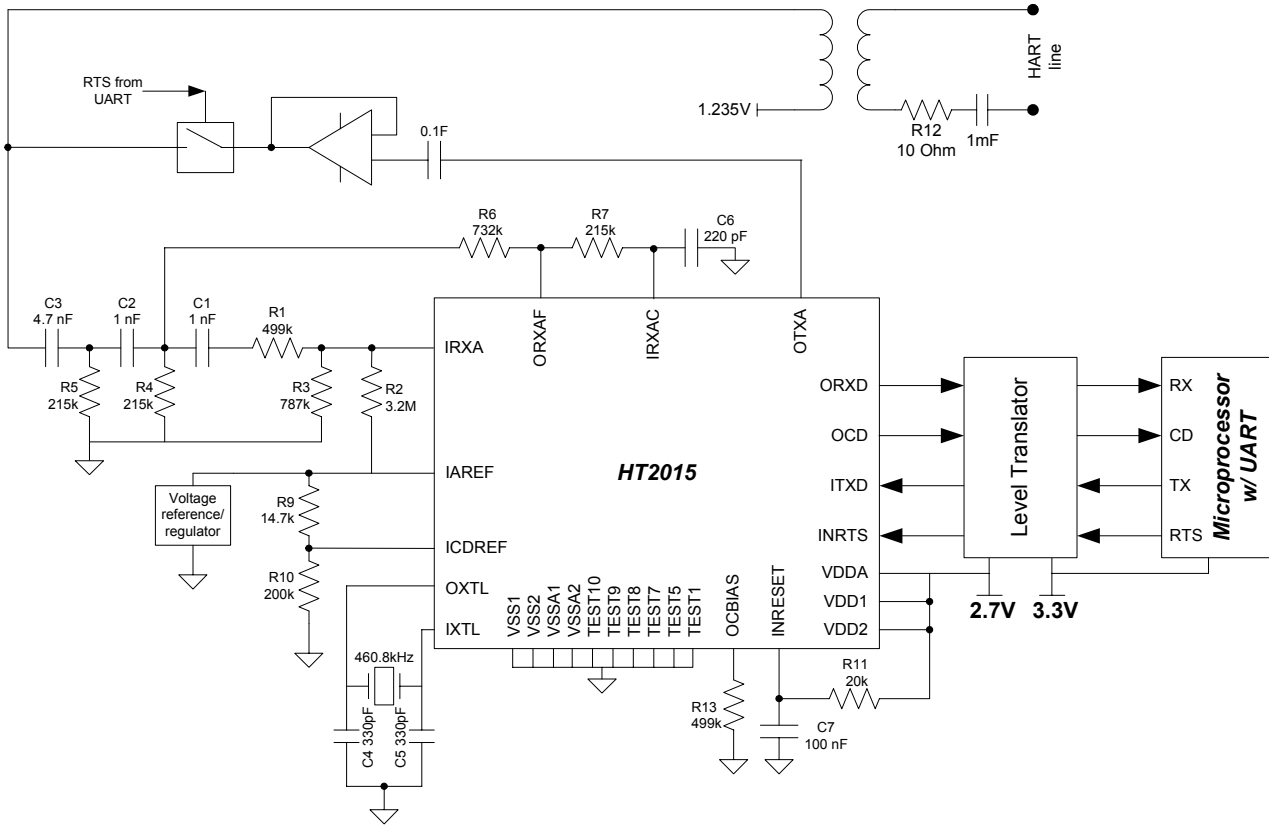


Figure 1 - HT2015 Test Design Overview Diagram

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