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Four Phase 40 Segment LCD Driver LCD160

Features:

- 160 segment driver
- Simple interface with microprocessor
- Bit to bit correspondence between input data and output drive or special SMAR decoding for SMAR LCD
- On chip back plane common signal generator
- 4.5V to 5.5V supply voltage
- 64 pin plastic QFP

LCD160 Four Phase 40 Segment LCD Driver

The LCD160 is an LCD driver that can directly drive up to 160 segments in the 1/4 duty cycle mode.

The LCD160 uses low power CMOS metal gate technology consisting of a 160 stage shift register, a 160 bit latch, a two mode encoder, 40 segments of LCD drive, and a four phase common signal generator. Display data is serially input to the SERDATA input and then to the 160 bit shift register synchronized with the SERCLK clock. The data is

transferred to the 160 bit latch by the LOAD signal. Latched data is then output to the 40 segment drivers in four phases. The MODE pin determines the mode selection; either a straight connection when held low or when held high proprietary encode for SMAR designed LCDs.

The BACK (backplane) common signals are sequenced in four phases to provide the 160 segment drive.

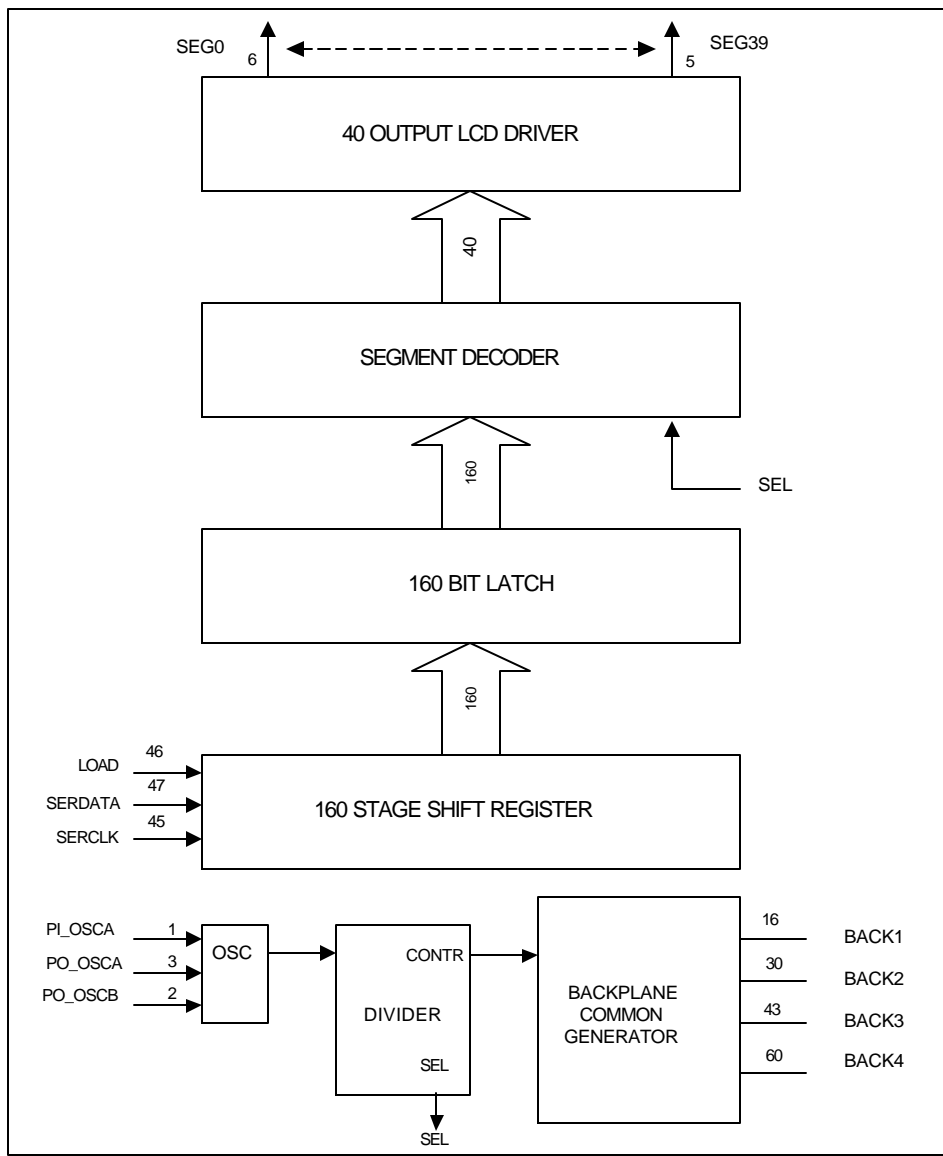


Figure 1 - Functional Block Diagram

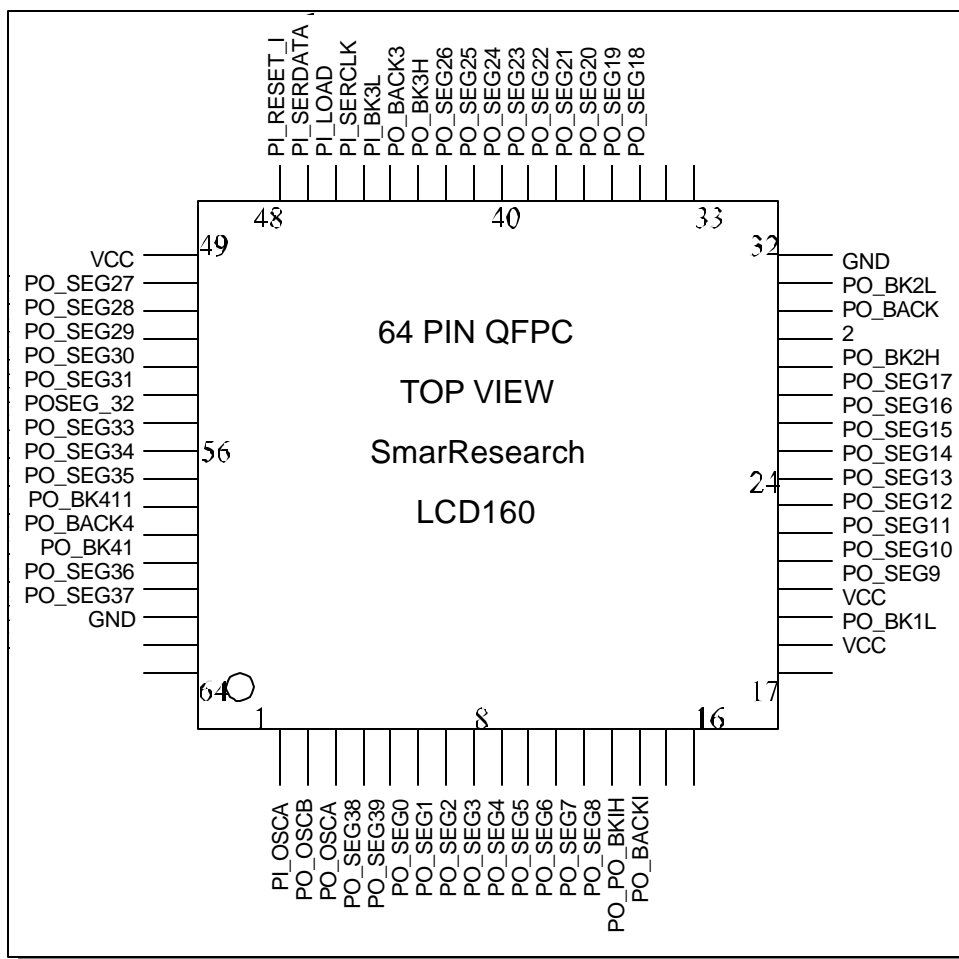


Figure 2 - LCD160 Pin Connections

PIN DESCRIPTION

PI_OSCA, PO_OSCA, PO_OSCB

By connecting the R0 and R1 external resistors plus the C0 external capacitor with PI_OSCA, PO_OSCA and PO_OSCB respectively as shown in figure 3 an oscillating circuit to generate the common backplane signals is formed. This frequency is divided by 1/8 by the internal dividing circuit, and is further divided by 1/4 to provide the common backplane signals.

The R1 resistor is used to limit the current on the PI_OSCA input terminal protecting diodes. The value of R1 should be 10 times that of R0.

MODE

When the MODE pin is held at a high level, the LCD160 operates in the SMAR display mode; when held at a low level in a one to one straight mode.

PI_SERCLK, PI_SERDATA

Display data is serially input from the PI_SERDATA pin to the 160 stage shift register at the rising edge of the PI_SERCLK pulse. The high level of the display data is used to turn the display on, while the low level of the display data is used to turn off the display.

PI_LOAD

The signal for latching the 160 stage shift register contents is input from this pin and occurs at the rising edge. When this pulse is present the shift register data is transferred to the 160 bit latch register.

PO_SEG0 - PO_SEG39

The LCD segment driving signals are output from these pins. They should be connected to the segment side of the display.

Depending on the MODE pin, the following signals produce these specific results:

- When a PO_BACK1 backplane common signal is generated the first 40 bits or a selected 40 bits is output to the segment drivers.
- When a PO_BACK2 backplane common signal is generated the second 40 bits or a selected 40 bits is output to the segment drivers.
- When a PO_BACK3 backplane common signal is generated the third 40 bits or a selected 40 bits is output to the segment drivers.
- When PO_BACK4 backplane common signal is generated the fourth 40 bits or a selected 40 bits is output to the segment drivers.

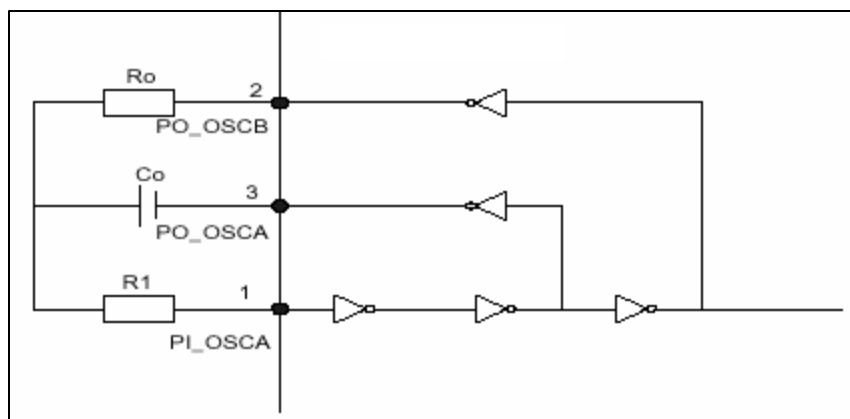


Figure 3 - LCD160 Internal Diagram

Operation

The LCD160 contains a 160 stage shift register, a 160 bit latch and 40 sets of segment drivers. The display data is input from the PI_SERDATA terminal to the 160 stage shift register at the rising edge of the PI_SERCLK pulse. It is transferred to the 160 bit latch on the rising edge of the PI_LOAD signal.

The data is output as the common backplane signals sequence, 40 segments at a time.

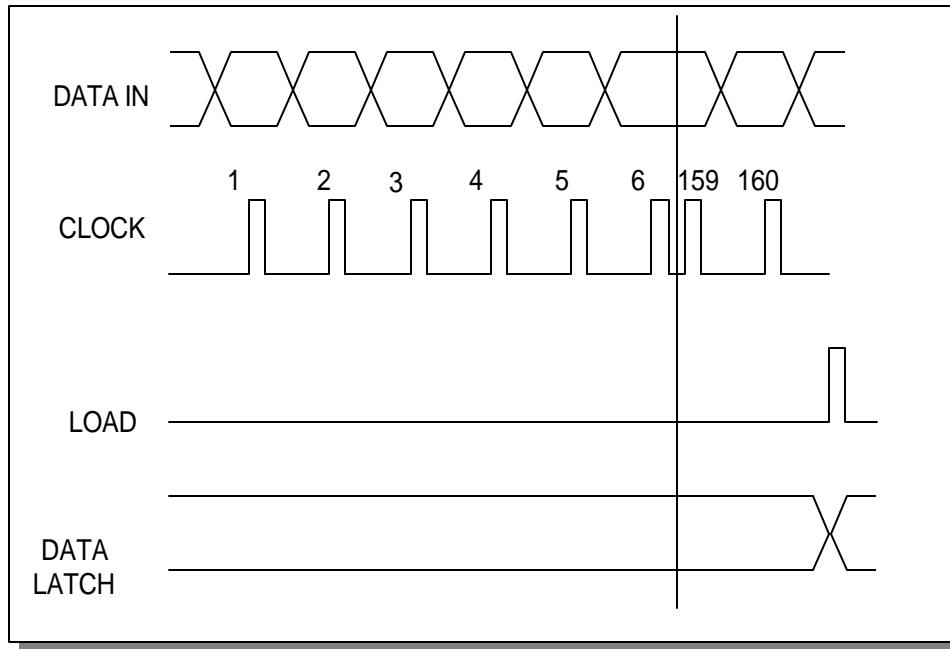


Figure 4 - Operation

Electrical Characteristics**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	Vdd	Ta=25°C	-0.3 to +6.0	V
Input Voltage	Vi	Ta=25°C	-0.3 to Vdd + 0.3	V
Storage Temperature	Tstg	-	-55 to +150	C

Operating Range

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	Vdd	-	4.5 to 5.5	V
Operating Temperature	Vop	-	-40 to +85	C
LCD Driving Voltage	Vss-Vdd	-	0 to 5	V
LCD Middle Voltage	1/2Vss-Vdd	-	2.5	V

Reccomended Oscillator Cirsuit Values

Parameter	Symbol	Signal Pin	Conditrion	Min	TYP	MAX	Unit
Oscillator Resistance	Ro	p2 PO_OSCB	-		200		KΩ
Oscillator Capacitance	Co	p3 PO_OSCA	Film Capacitor		120		uF
Current Limit Resistance	R1	p1 PI_OSCA	R1>/= 10 Ro		2		MΩ
Common Backplane Signal Frequency	Fbak	p16 PO_BACK1 p30 PO_BACK2 p43 PO_BACK3 p60 PO_BACK4	-		55		Hz

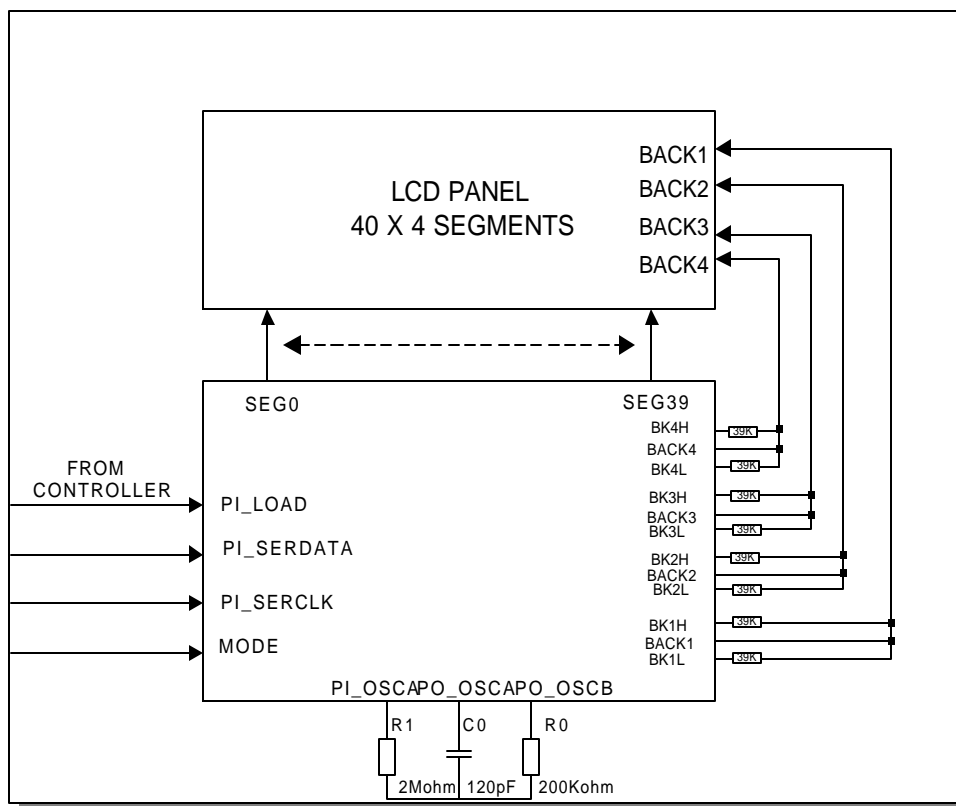


Figure 5 - Dynamic Display Mode Operation

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